NATIONAL INSTITUTE OF TECHNOLOGY KARNATAKA, SURATHKAL
राष्ट्रीय प्रौद्योगिकी संस्थान कर्नाटक, सुरत्कल
P.O SRINIVASNAGAR, MANGALORE - 575025

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EC Call Letter List

M Tech. (Research), 2023 - 24

The following applicants have been selected for written exam and/or interview for the department for the department of Electronics and Communication Engineering for M Tech. (Research) Programme. The applicants are requested to go through additional information provided in their Call letters.

#	Name	Reference Number	Branch/Specialisation
1	Mikkili Deepti	MTR2023SP0001	Signal Processing and Machine Learning
2	SUMANTH S P	MTR2023VL0002	VLSI Design
3	SUMANTH S P	MTR2023SP0002	Signal Processing and Machine Learning
4	Noel George	MTR2023VL0003	VLSI Design
5	ASHWINI NAGARAJ SHENOY	MTR2023SP0005	Signal Processing and Machine Learning
6	Ashutosh Chourey	MTR2023VL0004	VLSI Design
7	GORLE Shanmukha Narayana	MTR2023SP0009	Signal Processing and Machine Learning
8	Varun Kumar	MTR2023VL0006	VLSI Design
9	Vanlalpeka K Lalthazuali	MTR2023CN0002	Communication Engineering and Network
10	Arul Vignesh J	MTR2023VL0007	VLSI Design
11	ANJALI L	MTR2023VL0010	VLSI Design
12	ANJALI L	MTR2023CN0003	Communication Engineering and Network
13	RAMA GAUTAM	MTR2023VL0011	VLSI Design
14	Sagnik Ghosh	MTR2023VL0012	VLSI Design
15	RUTUJA PRASHANT TELANG	MTR2023VL0013	VLSI Design

23/5/23

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EC Call Letter List

M Tech. (Research), 2023 - 24

#	Name	Reference Number	Branch/Specialisation
16	Surya Narayanan S	MTR2023CN0005	Communication Engineering and Network
17	Siddhali Vinodkumar Gadiya	MTR2023CN0006	Communication Engineering and Network
18	Siddhali Vinodkumar Gadiya	MTR2023VL0014	VLSI Design
19	Nehasri Jonnadula	MTR2023VL0015	VLSI Design
20	SOURAV SARKAR	MTR2023VL0016	VLSI Design
21	SOURAV SARKAR	MTR2023SP0013	Signal Processing and Machine Learning
22	SOURAV SARKAR	MTR2023CN0007	Communication Engineering and Network
23	HIMANSHU KOLEY	MTR2023VL0019	VLSI Design
24	HIMANSHU KOLEY	MTR2023SP0016	Signal Processing and Machine Learning
25	HIMANSHU KOLEY	MTR2023CN0009	Communication Engineering and Network
26	TADEPALLI VENKATA KOMALESH	MTR2023VL0020	VLSI Design
27	Ranjana Prasad	MTR2023VL0021	VLSI Design
28	Anurag Anand	MTR2023VL0022	VLSI Design
29	Shivendra Pratap	MTR2023VL0023	VLSI Design
30	NABARUN DAS	MTR2023VL0025	VLSI Design
31	S P SREEJAN	MTR2023VL0026	VLSI Design
32	NABARUN DAS	MTR2023SP0018	Signal Processing and Machine Learning
33	ASHWIN GEO JOLLY	MTR2023VL0029	VLSI Design
34	THATIKONDA GOPAL RAO	MTR2023VL0030	VLSI Design
35	Devendra Singh	MTR2023VL0031	VLSI Design

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EC Call Letter List

M Tech. (Research), 2023 - 24

#	Name	Reference Number	Branch/Specialisation
36	ANUP KUMAR	MTR2023VL0032	VLSI Design
37	Arunachaleashwer S	MTR2023SP0020	Signal Processing and Machine Learning
38	Manivannan S	MTR2023SP0022	Signal Processing and Machine Learning

23/5/23

Head Of Department
Electronics and Communication Engineering

Department of Electronics & Communication Engineering ★ National Institute of Technology Karnataka, Surathkal ★ P.O. Srinivasnagar, Mangalore - 575 025. KARNATAKA, INDIA

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
NATIONAL INSTITUTE OF TECHNOLOGY KARNATAKA SURATHKAL
P.O. SRINIVASNAGAR, MANGALURU-575 025
Telephone: 0824-2473046, Website: www.ece.nitk.ac.in

Date: 24-05-2023

Shortlisted candidates for M Tech (R/S) Programme–Written Aptitude Test / Interview for the year 2023-24

With reference to your application for admission to M Tech (R/S) Programme in the department of Electronics and Communication Engineering, you are requested to appear for the Written test/Interview at NITK Surathkal. You should produce all the original records such as Date of Birth Certificate, GATE Score Card, Degree Certificate and Marks Cards of all semesters (UG programme), SC/ST/OBC/EWS certificate (if applicable as per proforma), Person with disability certificate (if applicable), Sponsorship letter (if applicable), Conduct Certificate and valid photo identity card. Please keep a self-attested photocopy of all these certificates readily available at the time of interview.

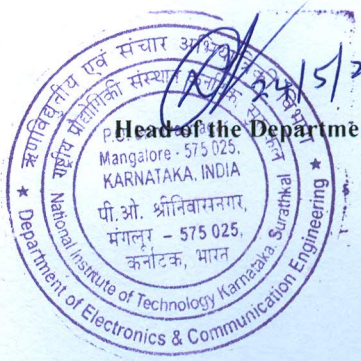
Department	: Department of Electronics and Communication Engineering
Place of Reporting	: Department of Electronics and Communication Engineering, NITK Surathkal
Written Test Date and Time	: June 19, 2023, 9.00 AM at ECE Department
Announcement of shortlisted candidates for interview	: June 19, 2023, 12.00 PM
Interview Date and Time	: June 19, 2023, 2.00 PM Onwards, Meeting room, ECE Department June 20, 2023, 9.00 AM Onwards, Meeting room, ECE Department

NOTE:

1. Candidates should be prepared to appear for a written Aptitude Test before the interview.
2. Candidates should be prepared to appear for the written Aptitude Test before the interview. Fee Structure for M Tech (S/R) programme and Course syllabus are provided on Institute's website, i.e. www.nitk.ac.in. A copy of the syllabus for the aptitude test is given in a separate page.
3. Full-time/External Registrants - sponsored from Industry or other organizations, should have been serving in the sponsoring organisation for a period of **at least 2 years** after qualifying degree and have to produce a letter from their employer stating that the candidate is deputed for M Tech / M Tech (Research) in the Institute on full salary during the study period. The employer should indicate that the candidate will not be withdrawn midway before the completion of the course. (Sponsorship letter should be in the format provided in the Application Form).
4. Candidates who have not submitted marks of final examination along with application form shall produce the same at the time of admission if available.
5. Your candidature for this test is provisional & is subject to your fulfilling the educational qualifications & other criteria prescribed for the programme as mentioned in the Information Brochure, failing which your candidature can be summarily rejected after verification/scrutiny at a later stage.
6. Please keep the Admit Card ready during the offline test and interview. You are responsible for safe custody of the Admit Card and in the event of any other person using this Admit Card, the responsibility lies on you to prove that you have not used the service of an impersonator.
7. Please note that no expenses shall be payable for appearing in the written test/Interview.

24/5/2023

Head of the Department



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Date: 24-05-2023

Syllabus for M. Tech. (Research) Aptitude Test- June 2023

The Test paper has 2 Parts, Part-1 is compulsory, and Part-2 is stream specific modules. The candidate is supposed to attempt Module A or Module B or Module C from Part-2 depending on the candidature for a particular M. Tech(R) streams. Part-1 has 15 multiple choice type questions, whereas, each module of Part-2 has 15 multiple choice type questions. Each correct answer carries 1 mark and wrong answer carries -0.25 marks.

Note: Total duration of Exam is one hour. Calculator is permitted.

Part-1:

Linear Algebra, Calculus, Differential and Difference equations. Numerical methods, Transforms, Linear circuits and networks, Electronic components and Devices, Analog Electronics, Digital Electronics, Signals and Systems, Linear and Digital Control Theory.

Part-2:

Module-A (CEN Stream)

Electromagnetic Waves, Probability and Random Processes, Communication Theory, Communication Circuits, Transmission Lines, Wave Guides, Antennas, Microwave devices and Circuits, Data Communications, Communication Networks, Satellite Communication, Optical Communication, Fundamentals of Signal Processing.

Module-B (SPML stream)

SP Fundamentals: Time domain analysis of discrete-time systems - Basic discrete time signals, discrete-time Fourier Series, Z Transform – definition and properties, Discrete-time Fourier Series and its properties, Properties and applications of DTFT. Relationship between time, Z and frequency domains, DFT fundamentals and Properties of DFT, FIR and IIR filters.

Data Structure Fundamentals: Algorithm analysis, Asymptotic notations. Divide and Conquer algorithms, Analysis of divide and conquer algorithms, master method, examples - merge sort, quick sort, binary search, Data structures, Linked list, stacks and queues.

Module-C (VLSI Design)

Linear and Digital ICs, Digital System Design, VLSI Technology, CMOS VLSI, Mixed Signal Design, HDL, Data converters, Microprocessors, Computer Architecture and organization, Logic Synthesis, DSP Architectures, Embedded Systems.