

Date: 03-06-2022

Syllabus for M. Tech. (Research) Aptitude Test- June 2022

The Test paper has 2 Parts, Part-1 is compulsory, Part 2 is stream specific modules. The candidate is supposed to attempt Module A and/or Module B and/or Module C from Part-2 depending on the candidature for a particular M. Tech. Streams. Part-1 has 15 multiple choice type questions, whereas, each module of Part-2 has 10 multiple choice type questions. Each correct answer carries 1 mark and wrong answer carries – 0.25 marks.

Part-1: Time: 30 Minutes

Linear Algebra, Calculus, Differential and Difference equations. Numerical methods, Transforms, Linear circuits and networks, Electronic components and Devices, Analog Electronics, Digital Electronics, Signals and Systems, Linear and Digital Control Theory

Part-2: Maximum marks for each module: 10 marks and time allocated for each module: 20 Minutes

Module-A (CEN Stream)

Electromagnetic Waves, Probability and Random Processes, Communication Theory, Communication Circuits, Transmission Lines, Wave Guides, Antennas, Microwave devices and Circuits, Data Communications, Communication Networks, Satellite Communication, Optical Communication, Fundamentals of Signal Processing.

Module-B (SPML stream)

SP Fundamentals: Time domain analysis of discrete-time systems - Basic discrete time signals, discrete-time Fourier Series, Z Transform – definition and properties, Discrete-time Fourier Series and its properties, Properties and applications of DTFT. Relationship between time, Z and frequency domains, DFT fundamentals and Properties of DFT. FIR and IIR filters.

Data Structure Fundamentals: Algorithm analysis, Asymptotic notations. Divide and Conquer algorithms, Analysis of divide and conquer algorithms, master method, examples - merge sort, quick sort, binary search, Data structures, Linked list, stacks and queues.

Module-C (VLSI Design)

Linear and Digital ICs, Digital System Design, VLSI Technology, CMOS VLSI, Mixed Signal Design, HDL, Data converters, Microprocessors, Computer Architecture and organization, Logic Synthesis, DSP Architectures, Embedded Systems.

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3-6-2022 Department
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